

REMARKS

I. Introduction

In response to the Office Action dated May 31, 2006, Applicants have amended claims 2 and 4, and canceled claims 1, 3, and 5 – 7. No new matter has been added. In view of the foregoing amendments and the following remarks, Applicants respectfully submit that all pending claims are in condition for allowance.

II. Claim Rejections Under 35 U.S.C. § 112

Claim 7 was rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite. Applicants have canceled claim 7. Accordingly, this rejection is now moot.

III. Claims Rejections Under 35 U.S.C. §§ 102 and 103

Claims 1 and 5 – 7 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. 4,910,735 to Yamashita. Claims 2 – 4 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Yamashita in view of U.S. Patent No. 5,157,781 to Harwood. Claims 1, 3, and 5 – 7 have been canceled by this amendment and as such these rejections are now moot. Applicants traverse the rejections of claims 2 and 4 for at least the following reasons.

Claims 2 and 4 each recite, among other things, an instruction converting device between the pseudorandom number generating device and the input switchover device outputting the pseudorandom numbers without change when the pseudorandom numbers inputted from the pseudorandom number generating device are defined instructions, and converting the pseudorandom numbers into the defined instructions when the pseudorandom numbers are undefined instructions to thereby output the defined instructions. At least this feature is not disclosed or suggested by Yamashita or Harwood, alone or in combination with each other.

According to one embodiment of the invention, instructions are implemented using pseudorandom numbers. When the pseudorandom numbers are undefined instructions, the processor may implement exception processing, which requires a longer testing time. As recited in claims 2 and 4, an instruction converting device is provided wherein pseudorandom numbers representing undefined instructions are first converted into defined instructions. Accordingly, it becomes unnecessary for the processor to implement the exception process, thus improving the activation rate. Additionally, fault detection with a high fault detection rate and fault detections at the actual operating speed can both be achieved.

The Examiner correctly acknowledges that Yamashita fails to disclose an instruction converting device and relies on Harwood to overcome this deficiency. However, Harwood merely discloses a method for performing a scan test. In Harwood, a system integration module (16) provides a method of interfacing an inter-module bus (12) to an external bus (17). The system integration module (16) contains a test module (18) which performs scan based testing of various modules within the system. Importantly, however, Harwood does not even suggest an instruction converting device that converts pseudorandom numbers representing undefined instructions into defined instructions.

Accordingly, as each and every limitation must be disclosed or suggested by the cited prior art references in order to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 (see, M.P.E.P. § 2143.03), and neither Yamashita nor Harwood, alone or in combination with each other does so, it is respectfully submitted that claims 2 and 4 are patentable over these references.

IV. Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If

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there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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